

Tools for Moving AltiVec DSP Applications to Intel Processors

Agenda

Conversion Challenges

Tools

Schedule

Beta Testing

Conversion Challenges

Problem:

AltiVec roadmap products are uncertain

Opportunity:

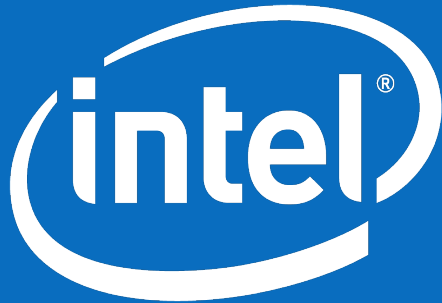
Intel® multicore processors are very effective for DSP applications

BUT: Converting existing, highly optimized AltiVec software to IA SSE can be a daunting task

- Time and Resources
- Performance Issues

Software is biggest hurdle

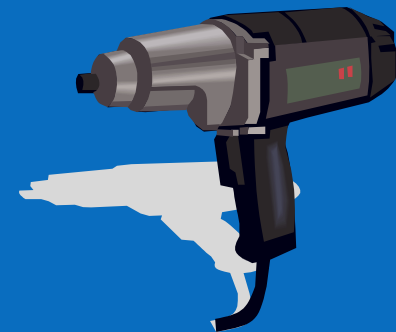
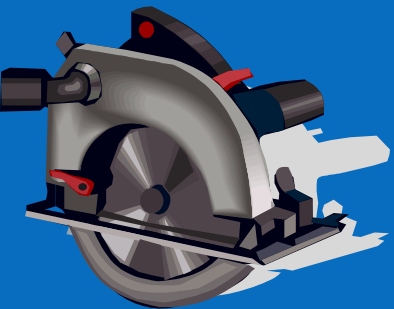
Tools



VSIPPL Library for IA

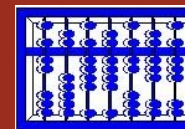
AltiVec.h Header File for IA

AltiVec Assembler Compiler for IA



N A Software tools for Intel Architecture Processors

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Vector Signal Image Processing Library

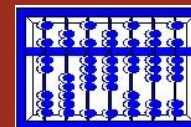


- Highly efficient computational middleware for signal and image processing applications
- Application programming interface (API) defined by the VSIPL Forum*
 - Open standard group -- embedded signal and image processing hardware and software vendors, academia, application developers, government labs
 - <http://www.vsipl.org/>
- Abstracts hardware implementation details; applications are portable across processor types and generations

- Standard API allows you to capture customers from other hardware platforms
- Hides hardware details; allows upgrades to a system without rewriting the software
- Software that uses portable interfaces can evolve over time more efficiently than low-level code designed for one architecture
- *However, we're agnostic: if your users don't like VSIPL, we can provide them with “plain C” CSIPL or convert your in-house libraries to IA*
 - We develop DSP performance libraries using “Liberator”, a proprietary semi-automated tool: Maintains efficiency but cuts the cost of providing new APIs

Examples:

- Optimised FFTW FFT library for IA
- CSIPL: “plain C” equivalent of VSIPL for IA
- Customers’ in-house DSP libraries ported to IA

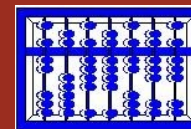


VSIPL standard defines subsets (profiles)

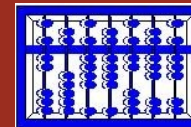
- Core Lite – 127 functions
- Core – 511 functions
- Full VSIPL (I haven't counted)
- Image – image processing add-on

NASL VSIPL supports “Core Plus” (almost full VSIPL);
single precision (32 bit) reals

Image Processing extension: almost ready (Jan09)



- Histogram Operations
- Convolution
- Diff / Edge Detection
- Image Pad
- Arithmetic Operations
- Logical Functions
- Morphological Operations
- Image Resize
- Object Functionality (e.g., bind/rebind)
- Conversion

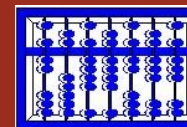


Tool 1: VSIPL Library for IA

DSP portion of application remains unchanged

Recompile target application with NASL VSIPL library; VSIPL calls execute automatically on Intel® processors

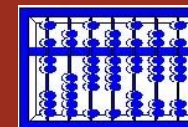
- “Core” Profile coverage at beta release
 - Complex-to-complex, real-to-complex, complex-to-real single and multiple 1D FFTs, filters/other DSP functions; vector/matrix functions; linear algebra
 - Product release will be Full VSIPL including 2D FFTs
 - Based on NASL PowerPC VSIPL Library
 - Supports Intel SSE2-SSE4 processors
 - Fully multithreaded
 - Aims to match or beat efficiency of Intel Math Kernel Library™
 - NASL-funded; Intel expedited
- Linux* Beta (2.6 kernel) release for testing and POCs available now
 - VxWorks* 6.6 SMP Beta release for testing and POCs available now



Beta Tool 1 (Linux) Sample Timings (μ secs) ccfftip

Intel "Caneland" Server; 4x 1.86 GHz Xeon Processors; Linux 2.6 kernel

N	NA Software C + Assembly	Intel MKL (Assembly)
16	0.11	0.12
32	0.14	0.16
64	0.25	0.30
128	0.51	0.55
256	1.2	1.1
512	2.7	2.5
1024	5.7	5.2
2048	14.4	13.3

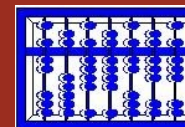


Beta Tool 1 (Linux) Performance

N=1024 FFT Timings (microseconds)

Routine	PPC	Intel
Real to Complex	7.5	4.5
Complex to Real	7.7	4.6
Complex to Complex out of place	10.9	6.8
Complex to Complex In Place	10	6.5

PPC: 8641D@1GHz, 400MHz bus
IA: Core Duo 2 @ 2.16GHz
NAS Intel VSIPL beta release (Linux)

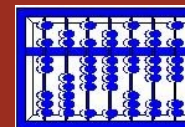


Beta Tool 1 (Linux) Performance

N=1024 Vector Routines (microseconds)

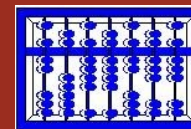
Routine	PPC	IA
Vector Square root	1.4	1.3
Complex vector multiply	2.4	1.8
Vector multiply & add	1.4	0.7
Polar Convert	15.6	10.7
Vector Cosine	3	6.4

PPC: 8641D@1GHz, 400MHz bus
IA: Core Duo 2 @ 2.16GHz
NAS Intel VSIPL beta release (Linux)



Tool 1: Evaluation and Licensing

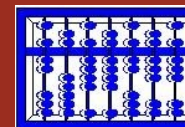
- **Beta evaluation copies for Tool 1 are available free of charge**
- **Support will be handled directly through NA Software Ltd.**
- **NA Software Ltd. owns the intellectual property for the IA VSIPL library code**
 - **Licensing for the Gold Release of Tool 1 will be handled directly by NA Software Ltd**
 - **Support will be handled directly through NA Software Ltd.**



Tool 1: Gold Product Release

- **Full VSIPL profile**
- **Single precision, 1D +2D FFTs**
- **Faster FFTs**
- **Available for licensing from NASL: January, 2009**
- **CSIPL “Plain C” API also available**

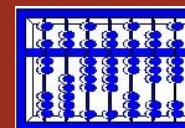
All dates, product descriptions, availability and plans are forecasts and subject to change without notice



Tool 2: `altivec.h` Header File for IA

- “`altivec.h`”: `#include` file often used by PowerPC* DSP software to access AltiVec* SIMD functionality
 - NASL’s `altivec.h` is a replacement include file targeting IA
 - Application’s DSP code remains unchanged
 - Recompile target application with new `altivec.h` file; AltiVec SIMD instructions automatically converted to SSE SIMD code
 - Supports Intel SSE2-SSE4 processors
 - Fully multithreaded
 - Intel funded; available from NASL
- Linux Beta for testing and POCs available now**
- VxWorks 6.6 SMP Beta version planned January, 2009
 - Gold Release Schedules (tentative)
 - Linux: January 1st 2009
 - VxWorks 6.6: March 2009

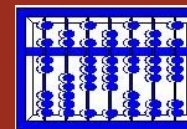
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Tool 2: Evaluation and Licensing

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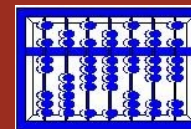
- **Support will be handled directly through NA Software Ltd.**
- **Intel owns the intellectual property for the Altivec.h→ SSE conversion utility**
 - Tool has been funded by Intel
 - Intel can provide the Gold Altivec.h tool to customers at no charge
 - Long-Term support would have to be negotiated directly with NA Software Ltd.
 - Intel is also discussing other RTOS versions and long-term support possibilities with several important RTOS vendors



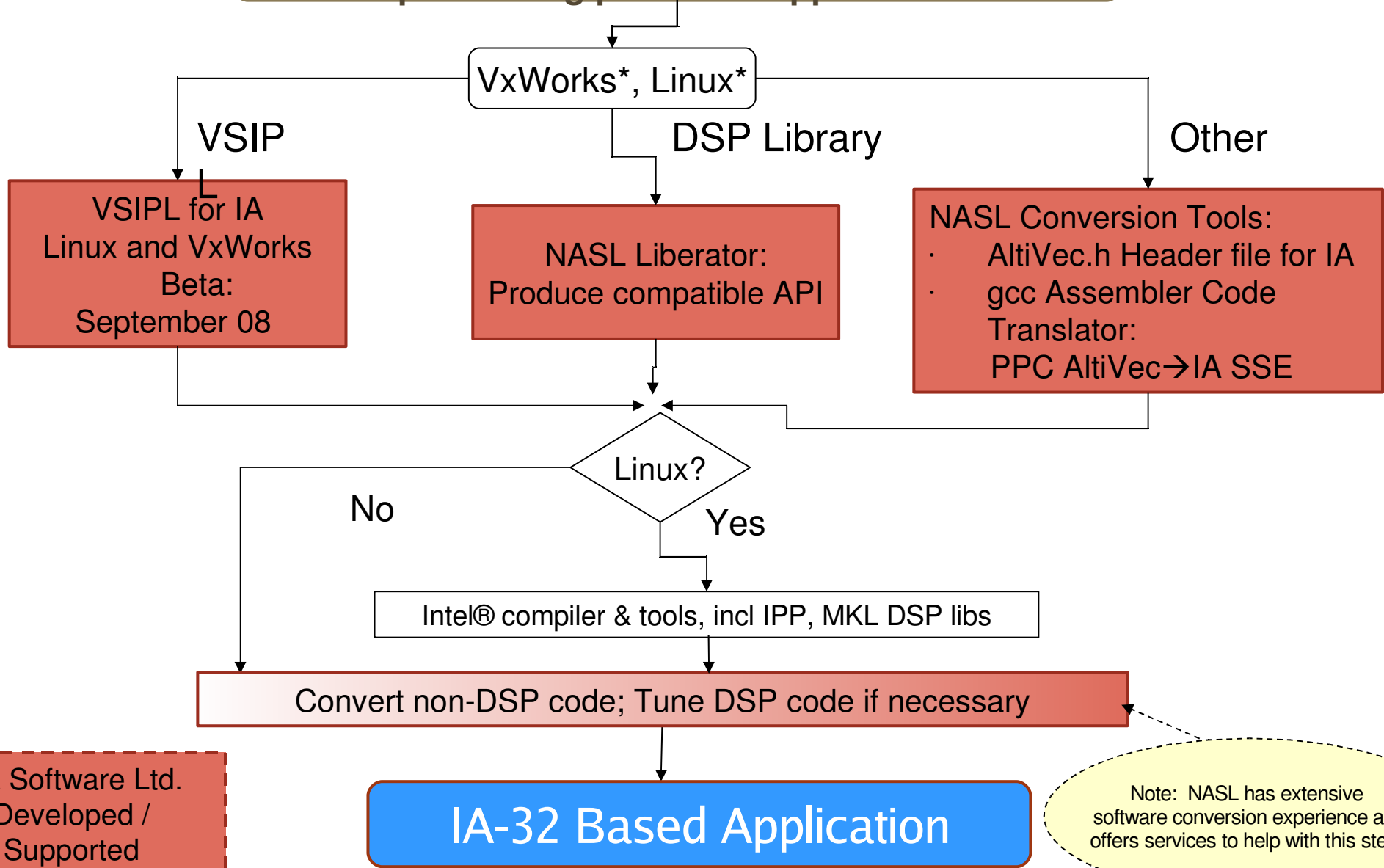
Tool 3: AltiVec Assembler Compiler for IA

- **Input: PPC AltiVec assembler code**
 - Utility builds internal representation of object code
 - Feeds into gcc's back-end optimization and object code generation functionality
- **Output: Intel SSE assembler code**
- **Initial feasibility design study under way**
 - Prototype Alpha version and report due end of 2008
- **If successful: VxWorks and Linux Beta product could release in mid 2009**
- **Intel funded; available from NASL**

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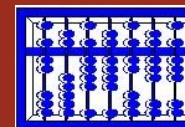


AltiVec*-based signal & image processing portion of application



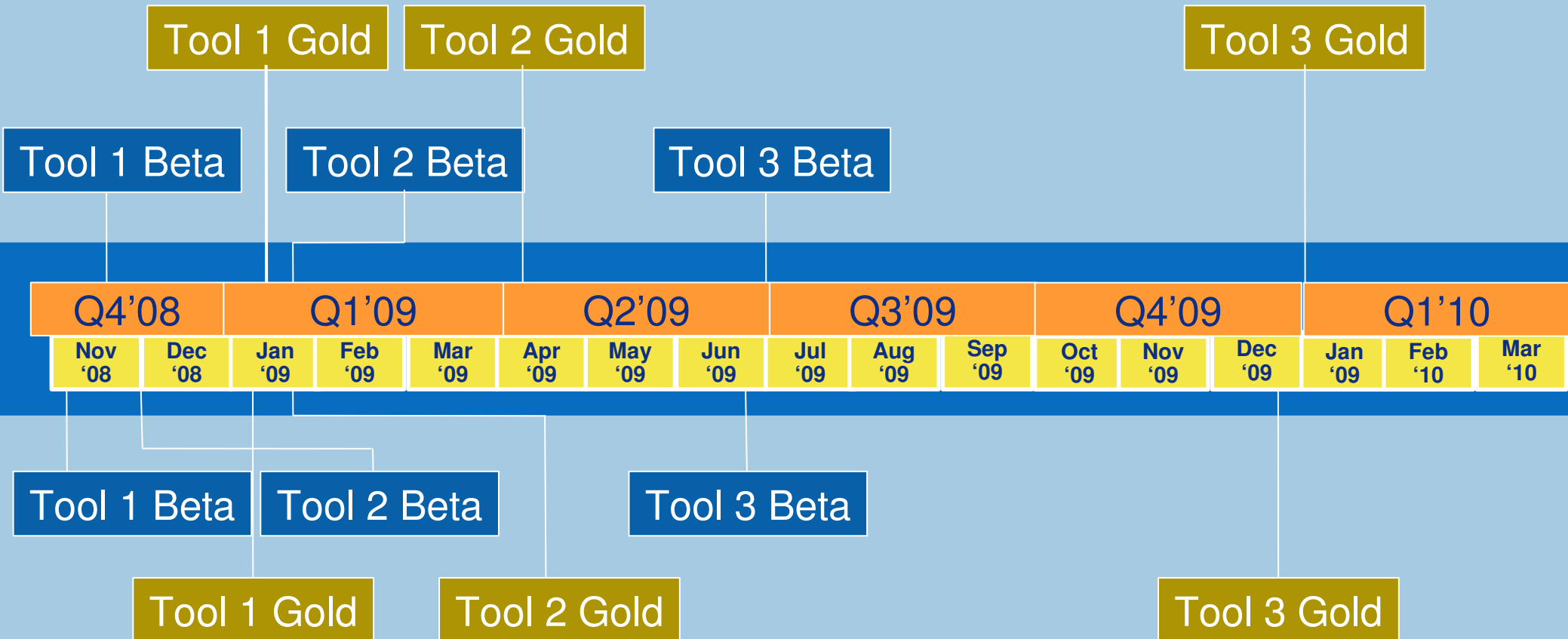
NA Software Ltd.
Developed /
Supported

Note: NASL has extensive software conversion experience and offers services to help with this step



Tools Release Schedule

VxWorks 6.6



Linux (2.6 Kernel)

Tool 1 - VSIPL Library for IA

Tool 2 - AltiVec.h Header File for IA

Tool 3 - AltiVec Assembler Compiler for IA

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Summary

- Intel processors are very effective for DSP workloads
- Three Tools from NA Software to simplify conversion
- Join the Beta Testing program



More Information

Mike Delves: delves@nasoftware.co.uk

NA Software Ltd.

1 Prospect Road

Birkenhead, CH42 8LE

U.K.

+44 151 609 1911

FAX: +44 151 550 7830

Peter Carlston: peter.carlston@intel.com

Intel Corporation

CH6-236

5000 W. Chandler Blvd.

Chandler, Arizona 85226

